Set	Items	Description
S1	59882	(ERROR? ? OR PARITY)(3N)(CHECK??? OR EXAM? OR TEST??? OR D-ETECT? OR ANALYZ? OR ANALYS?)
S2	94249	(SECOND? OR 2ND OR TWO OR SEPARAT? OR DIFFERENT OR ANOTHER OR OTHER)(5W)(MEMORY OR MEMORIES OR RAM OR STORE OR STORES OR STORAGE)
S3	107531	MULTIPLEX?
S4	64	S1 AND S2 AND S3
S5	1010	S2(20N)S3
S6	30	S4 AND S5
S7	30	IDPAT (sorted in duplicate/non-duplicate order)
S8	3397	DUAL?(5W)(MEMORY OR MEMORIES OR RAM OR STORE OR STORES OR - STORAGE)
S9	0	S8(20N)S3 AND S1

DIALOG(R)File 350:Derwent WPIX
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011115634   **Image available**
WPI Acc No: 1997-093559/199709
XRPX Acc No: N97-077438
  **SOH termination circuit for SOH wireless transmission system – has RSOH
  multiplexer which multiplexes signals input from MSOH multiplexer
  and outputs multiplexed STM-N signal**
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
JP 8331088   A   19961213 JP 95152507   A   19950526 199709 B

Priority Applications (No Type Date): JP 95152507 A 19950526
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
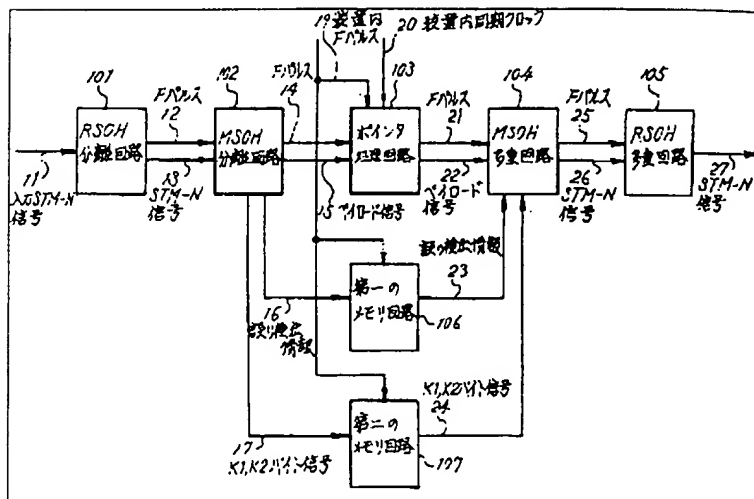JP 8331088   A   5 H04J-003/08

Abstract (Basic): JP 8331088 A
     The circuit consists of a RSOH separation unit (101) to which a
composite STM-N signal (11) is input. This unit establishes frame
synchronization and separates input signal as descramble signal (12)
and STM-N signal (13). Then, an MSOH separation unit (102) separates
input signal further as MSOH signal (16) and is output to a first
memory unit (106) and K1 and two bytes of Ks signal for **error
detection** is given to a **second memory** unit (107). F pulse (19)
from an external device is also fed to the first and **second memory**
units and to a pointer processing unit (103). The MSOH separation unit
outputs frame pulse (14) and a pay load signal (15) to the pointer
processing unit in synchronization with clock signal (20) from an
external device. The output signals (23,24) of the first and **second
memory** units is fed to an MSOH **multiplexer** (104).
     The output frame pulse (21) and processed pay load signal (22) from
the pointer processing unit is also fed to the MSOH **multiplexer** . When
the bit interleave parity signal output from **second memory** unit
differs from the signals K1 and two bytes of Ks for **error detection**
, the corresponding **parity** bit of the pay load signal is inverted.
The **multiplexed** outputs (25,26) from the MSOH **multiplexer** is fed to
an RSOH **multiplexer** (105) which **multiplexes** RSOH and scramble
signals and outputs **multiplexed** STM-N signal.
     ADVANTAGE - Enables ring protection between STM-N **multiplexes** in
SDH wireless transmission system.
     Dwg.1/2

Title Terms: TERMINATE; CIRCUIT; WIRELESS; TRANSMISSION; SYSTEM; **MULTIPLEX**
  ; **MULTIPLEX** ; SIGNAL; INPUT; **MULTIPLEX** ; OUTPUT; **MULTIPLEX** ; STM; N;

SIGNAL
Derwent Class: W02
International Patent Class (Main): H04J-003/08
International Patent Class (Additional): H04J-003/00
File Segment: EPI
Manual Codes (EPI/S-X): W02-K02; W02-K02B3

7/19/6   (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013009867   **Image available**
WPI Acc No: 2000-181719/200016
XRPX Acc No: N00-134136
   **Data access method for values stored in cache of computer, in which dual
   associative-cache directories are configured to allow simultaneous read
   operation using two buses with** multiplexers
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC   )
Inventor: ARIMILLI R K; DODSON J S; LEWIS J D; SKERGAN T M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6023746	A	20000208	US 97839558	A	19970414	200016	B

Priority Applications (No Type Date): US 97839558 A 19970414
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6023746	A		12	G06F-012/00	

Abstract (Basic): US 6023746 A
      NOVELTY - Dual associative-cache directories allow simultaneous
read operations using **two** buses with **multiplexers** , address tags,
memory block control signals, single clock cycle operation and error
correction.
      DETAILED DESCRIPTION - The method involves accessing values stored
in a cache used by a processor, such that **two** read operations may
occur simultaneously. **Memory** blocks from a memory device are loaded
into respective cache lines of the cache memory, and address tags
associated with the memory blocks are written into two redundant cache
directories of the cache. Memory blocks can then be read from the cache
using either of the two cache directories. INDEPENDENT CLAIMS are
included for; a computer system with cache memory access mechanism for
accessing values stored in a cache.
      USE - Dual associative-cache directories for simultaneous read
operation, in which read operations may occur simultaneously.
      ADVANTAGE - Provide cache that efficiently uses all available cache
lines without excess logic circuits in the critical path. Improved
handling of defects, including defect avoidance and error correction.
Provides cache having faster read access.
      DESCRIPTION OF DRAWING(S) - The drawing shows a high-level
schematic diagram of a set associative cache according to the
invention, with parity error control and dynamic repair mask.
      Set associative cache (70)
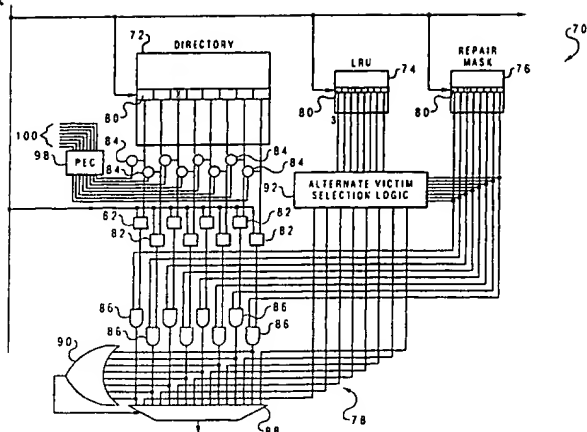   Cache directory (72)
      LRU array (74)
      Repair mask (76)
      Control logic (78)
      Comparators (82)
       Parity   checkers (84)
      pp; 12 DwgNo 3/4

Title Terms: DATA; ACCESS; METHOD; VALUE; STORAGE; CACHE; COMPUTER; DUAL;
   ASSOCIATE; CACHE; DIRECTORY; CONFIGURATION; ALLOW; SIMULTANEOUS; READ;
   OPERATE; TWO; BUS; **MULTIPLEX**
Derwent Class: T01
International Patent Class (Main): G06F-012/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-H03A; T01-M05

  7/19/7   (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012932609
WPI Acc No: 2000-104456/200009
XRPX Acc No: N00-080172
  Device for phase synchronization
Patent Assignee: PENZA TECHN INST (PETE-R)
Inventor: CHULKOV V A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RU 2119717	C1	19980927	RU 97106276	A	19970415	200009	B

Priority Applications (No Type Date): RU 97106276 A 19970415
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RU 2119717	C1			H03L-007/00	

Abstract (Basic): RU 2119717 C1
      NOVELTY - Device provides synchronization for reception of digital
   information and is based on direct automatic phase tuning without
   alternation of heterodyne frequency. Device has multiple-phase
   reference oscillator, which outputs are connected to information inputs
   of **multiplexer** . Goal of invention is achieved by introduced
   adder-subtracter, adder, bit-by-bit shift register, **two   memory**
   registers. One **memory** register has encoder and is reads phase of
   input signals. **Second   memory** register serves as digital filter
   together with adder-subtracter and bit-by-bit shift register. Current
   phase **error** is **detected** by adder operating in complementary code.
      USE - Communication.
      ADVANTAGE - Increased bandwidth of synchronization, increased speed
   of initiating synchronization, increased dynamic precision of
   synchronization. 1 dwge
      pp; 0 DwgNo 0/0
Title Terms: DEVICE; PHASE
Derwent Class: U22; U23; W01
International Patent Class (Main): H03L-007/00
International Patent Class (Additional): H04L-007/033
File Segment: EPI
Manual Codes (EPI/S-X): U22-H; U23-D; W01-A04B1

7/19/8   (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

012902172   **Image available**
WPI Acc No: 2000-074008/200007
XRPX Acc No: N00-057953
Sampling flip-flop for testing digital logic at end of production line
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC   )
Inventor: QURESHI F U R
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19927094	A1	19991230	DE 1027094	A	19990615	200007	B
KR 2000005741	A	20000125	KR 9919563	A	19990529	200063	
US 6182256	B1	20010130	US 9898236	A	19980616	200108	
DE 19927094	C2	20020221	DE 1027094	A	19990615	200213	
KR 327058	B	20020313	KR 9919563	A	19990529	200263	

Priority Applications (No Type Date): US 9898236 A 19980616
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19927094	A1		20	H03K-005/15	
KR 2000005741	A			H03K-019/00	
US 6182256	B1			G01R-031/28	
DE 19927094	C2			H03K-005/15	
KR 327058	B			H03K-019/00	Previous Publ. patent KR 2000005741

Abstract (Basic): DE 19927094 A1
     NOVELTY - The device has **two** temporary **memories** (918,920), each
with an input and output, and three **multiplexers** . The first
multiplexer (930) has a serial input, a parallel input, a selection
input and an output connected to the first memory's input. The second
multiplexer (940) has a serial input connected to that of the first
multiplexer , a flop input connected to the output of the first memory,
a selection input connected to that of the first **multiplexer** and an
output connected to the input of the **second memory** . The third
multiplexer (950) has inputs connected to the memory outputs, a
control input and an output.
     DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a
circuit with a chain of sampling flip-flops.
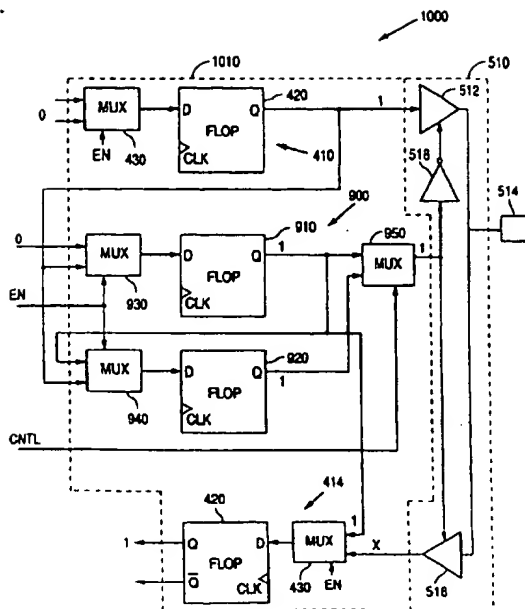   USE - For testing digital logic at the end of a production line.
     ADVANTAGE - **Test errors** caused by bi-directional connections
can be prevented.
     DESCRIPTION OF DRAWING(S) - The drawing shows a schematic block
diagram of a sampling flip-flop
     Temporary memories (918,920)
     Multiplexers (930,940,950)
     pp; 20 DwgNo 1/11

Title Terms: SAMPLE; FLIP; TEST; DIGITAL; LOGIC; END; PRODUCE; LINE
Derwent Class: S01; U21; U22
International Patent Class (Main): G01R-031/28; H03K-005/15; H03K-019/00
International Patent Class (Additional): G01R-031/3183
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01A5; U21-C03D1; U22-A04C; U22-D06

 7/19/9   (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

012887956   **Image available**
WPI Acc No: 2000-059790/200005
XRPX Acc No: N00-047015
  Frequency modulation multiplex **broadcast receiver for vehicle-mounted
  navigation system - has frame synchronization detection unit that detects
  timing by which frames of the** secondary **information are synchronized,
  and** memory **into which initial and secondary information are stored**
Patent Assignee: ALPINE KK (ALPN)
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
JP 11317679   A   19991116 JP 98121964   A   19980501 200005 B

Priority Applications (No Type Date): JP 98121964 A 19980501
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
JP 11317679   A   9 H04B-001/16
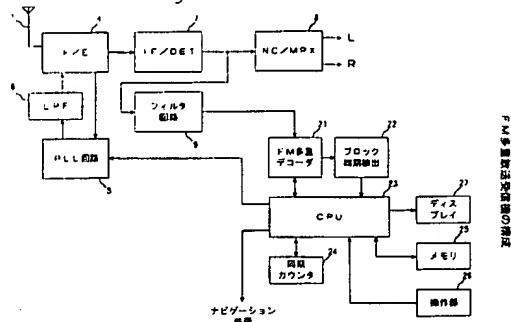
Abstract (Basic): JP 11317679 A
      NOVELTY - The synchronous block detector circuit detects the
   synchronization of the blocks contained in the secondary information
   demodulated by the FM **multiplex** decoder. A frame synchronization
   detection unit detects the timing by which the frames of the secondary
   information are synchronized, while the initial and **secondary**
   information are stored into a **memory** (25). DETAILED DESCRIPTION - A
   CPU (23) controls the frequency by which FM **multiplex** broadcasts are
   received by a broadcast receiver. An FM **multiplex** decoder (21) has a
   correction processor that corrects the errors of a synchronous block
   detector circuit (22) used in detecting synchronized blocks and the
   frame-synchronizing operations of a demodulator based on the initial
   information output from the broadcast receiver.
      USE - For vehicle-mounted navigation system.
      ADVANTAGE - Block and frame synchronization does not have to be

detected again even if receiving stations situated between FM
multiplex broadcast stations are switched. Errors in initial
information are reliably recovered using cyclic redundancy **check** ,
parity bits, or **parity** blocks. Reduces operating load of CPU.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the
FM **multiplex** broadcast receiver. (21) FM **multiplex** decoder; (22)
Synchronous block detector circuit; (23) CPU; (25) Memory.
Dwg.1/6

Title Terms: FREQUENCY; MODULATE; **MULTIPLEX** ; BROADCAST; RECEIVE; VEHICLE;
  MOUNT; NAVIGATION; SYSTEM; FRAME; DETECT; UNIT; DETECT; TIME; FRAME;
  SECONDARY; INFORMATION; MEMORY; INITIAL; SECONDARY; INFORMATION; STORAGE
Derwent Class: S02; T07; W02; W06
International Patent Class (Main): H04B-001/16
International Patent Class (Additional): G01C-021/00; G01S-005/14;
  G08G-001/09; G08G-001/0969
File Segment: EPI
Manual Codes (EPI/S-X): S02-B08; T07-B; W02-G03; W06-A03

 7/19/10   (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012588580   **Image available**
WPI Acc No: 1999-394687/199933
Related WPI Acc No: 1998-144927
XRPX Acc No: N99-295009
   Signal path error testing **method for pumped voltage gates in field
   programmable gate array**
Patent Assignee: XILINX INC (XILI-N)
Inventor: ERICKSON C R; MEHROTRA A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5920201	A	19990706	US 96588160	A	19960117	199933	B
			US 97935567	A	19970923		

Priority Applications (No Type Date): US 96588160 A 19960117; US 97935567 A
  19970923
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5920201	A		9	G01R-027/22	Div ex application US 96588160
					Div ex patent US 5717340

Abstract (Basic): US 5920201 A
     NOVELTY - A test signal and inverted test signal is supplied to the
  control transistors (504,505) respectively provided in the lines
  (502,503). Based on the signals, the memory cell (509) controls the
  pass gate to signal to line (513). The output signal is monitored on
  line to determine error in signal path.
     DETAILED DESCRIPTION - The memory outputs signal at a threshold
  voltage greater than the test signal voltage. Two inverters (506,507)
  are coupled in between the two lines. A configuration bit is stored in
  the **secondary memory** cell. Based on this bit the electrical signal
  is **multiplexed** between two lines. An INDEPENDENT CLAIM is also
  included for test circuit for testing a signal path.

USE - To determine the error in signal path for pumped voltage
    gates.
        ADVANTAGE - As three transistors and three **test** signals are used,
    error **detection** in signal path is faster.
        DESCRIPTION OF DRAWING(S) - The figure depicts the signal path
    error **testing** method from two local lines through a pass gate on to
    another line.
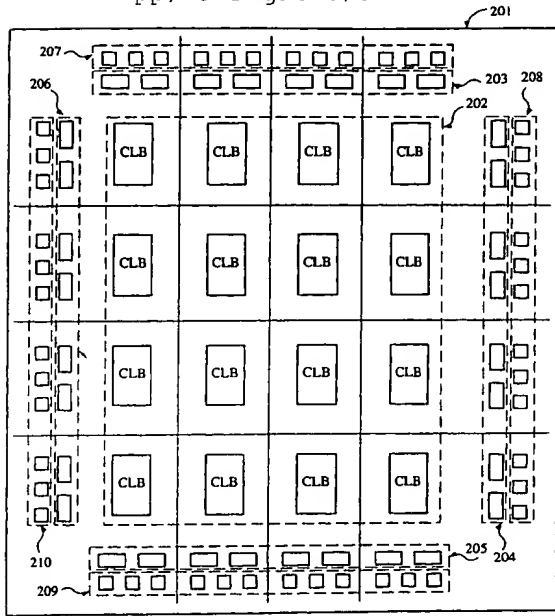   Lines (502,503)
        Inverter (506,507)
        Memory cell (501,509)
        Pass gate (508)
        Output line (513)
        pp; 9 DwgNo 5/5

Title Terms: SIGNAL; PATH; ERROR; TEST; METHOD; PUMP; VOLTAGE; GATE; FIELD;
    PROGRAM; GATE; ARRAY
Derwent Class: S01; U11; U13
International Patent Class (Main): G01R-027/22
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01A1; S01-G01A5; U11-F01C3; U13-C04D

 7/19/11   (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

011200801   **Image available**
WPI Acc No: 1997-178726/199716
XRPX Acc No: N97-147383
    Data **error** **detection** **and correction apparatus for shared SRAM -**
    includes two memories **divided into upper and lower regions which**
    store primary and backup information which are coupled to multiplexer
    and select logic which selects correct data
Patent Assignee: HONEYWELL INC (HONE); LORDI A L (LORD-I)
Inventor: LORDI A L
Number of Countries: 019 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5611042	A	19970311	US 95541989	A	19951010	199716	B
WO 9714109	A2	19970417	WO 96US16037	A	19961007	199721	
WO 9714109	A3	19970605	WO 96US16037	A	19961007	199737	
EP 862761	A2	19980909	EP 96937661	A	19961007	199840	
			WO 96US16037	A	19961007		
EP 862761	B1	19991222	EP 96937661	A	19961007	200004	
			WO 96US16037	A	19961007		
JP 11513823	W	19991124	WO 96US16037	A	19961007	200006	

Priority Applications (No Type Date): US 95541989 A 19951010
Cited Patents: 1.Jnl.Ref; US 4245344; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5611042	A		11	G01R-031/28	
EP 862761	B1	E		G06F-011/16	Based on patent WO 9714109

Designated States (Regional): DE FR GB

JP 11513823	W		23	G06F-012/16	Based on patent WO 9714109
DE 69605820	E			G06F-011/16	Based on patent EP 862761
					Based on patent WO 9714109
WO 9714109	A2	E	19	G06K-000/00	

Designated States (National): JP
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC
NL PT SE

EP 862761	A2	E		G06F-011/16	Based on patent WO 9714109

Designated States (Regional): DE FR GB

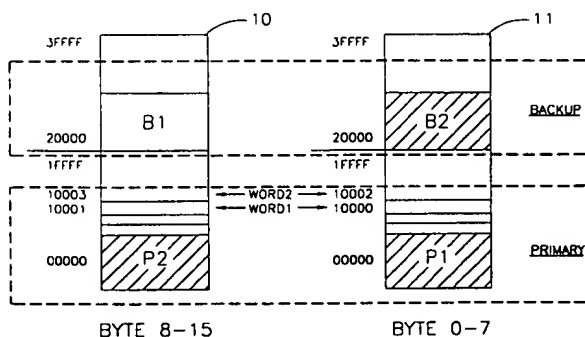|					
WO 9714109	A3			G01R-031/28	

Abstract (Basic): US 5611042 A

The memory information error correction apparatus includes **two memories** which are divided such that a lower memory stores primary information and an upper memory stores backup information. The upper memory addressable locations of the first memory correspond to relative addressable locations of the lower addressable memory locations of the **second memory** . A processor commands a simultaneous read of the primary information and the corresponding backup information. Memory select logic generates address information to cause the lower memories of the first memory and a corresponding relative address of the **second memory** to be read.

The primary information and the backup information is coupled to the input ports of a **multiplexer** . Select logic determines whether data in the **two memories** contains the primary or the backup information and generates a select signal to select the set of input ports containing the primary data when no error is indicated in the primary copy. The other ports are selected when an error is indicated in the primary copy and no error is indicated in the backup copy.

USE/ADVANTAGE - Error correction is performed without requiring additional time. For static random access memory.

Dwg.5/7

Title Terms: DATA; ERROR; DETECT; CORRECT; APPARATUS; SHARE; SRAM; TWO;
  MEMORY; DIVIDE; UPPER; LOWER; REGION; STORAGE; PRIMARY; INFORMATION;
  COUPLE; **MULTIPLEX** ; SELECT; LOGIC; SELECT; CORRECT; DATA
Derwent Class: S01; T01; U13; U14
International Patent Class (Main): G01R-031/28; G06F-011/16; G06F-012/16;
  G06K-000/00
International Patent Class (Additional): G06F-011/00; G11C-029/00
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01; T01-G03; T01-H01B; U13-C04B1B; U14-D02

DIALOG(R)File 350:Derwent WPIX

010468268
WPI Acc No: 1995-369587/199548
   Multiplexing **computer system for** error   detection   **- compares data
   read out from one memory with inverted data read out from** second
   memory **and judges disagreement in** multiplexing **system**
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7244612	A	19950919	JP 9433574	A	19940303	199548	B

Priority Applications (No Type Date): JP 9433574 A 19940303
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7244612	A		10	G06F-012/16	

Abstract (Basic): JP 7244612 A
      The **multiplexing** computer system synchronises functions of n
   number of elements. Each element has a calculating processing device
   and a memory which stores data of N bit width. The data transfer
   between the first calculating processing device (11-1) and the first
   memory (15-1) is done by first driver (18-1) through a first and second
   bus (17-1,12-1). Similarly the data transfer between second calculating
   processing device (11-2) and memory (15-2) is done by a second bus
   driver (18-2) through a third and fourth bus (17-2,12-2).
      The first bus driver transmits the data on the first bus to the
   second bus which carries data to the first processing device without
   changing the data. The second bus driver does level inversion of the
   data on the third bus and then transmits the level inverted data to the
   fourth which carries it to the second processing device. A comparison
   device (B) compares the data placed on the second and fourth bus and
   judges the abnormality in the **multiplexing** system.
      ADVANTAGE - Detects abnormality perfectly.
      Dwg.1/2
Title Terms: **MULTIPLEX** ; COMPUTER; SYSTEM; ERROR; DETECT; COMPARE; DATA;
   READ; ONE; MEMORY; INVERT; DATA; READ; SECOND; MEMORY; JUDGEMENT;
   MULTIPLEX ; SYSTEM   .
Derwent Class: T01
International Patent Class (Main): G06F-012/16
International Patent Class (Additional): G06F-011/16; G06F-011/18
File Segment: EPI
Manual Codes (EPI/S-X): T01-G01A; T01-G03

DIALOG(R)File 350:Derwent WPIX

010089948   **Image available**
WPI Acc No: 1994-357661/199444
XRPX Acc No: N94-280308
   Fibre optic distributed data interface network test adaptor error
   **injection circuit - injects errors into FDDI network to provide
   verification of operation of FDDI interface which can operate as network
   node with MAC identity**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: ECKENRODE T; STAUFFER D R; STEMPSKI R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5363379	A	19941108	US 92876835	A	19920430	199444	B

Priority Applications (No Type Date): US 92876835 A 19920430

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
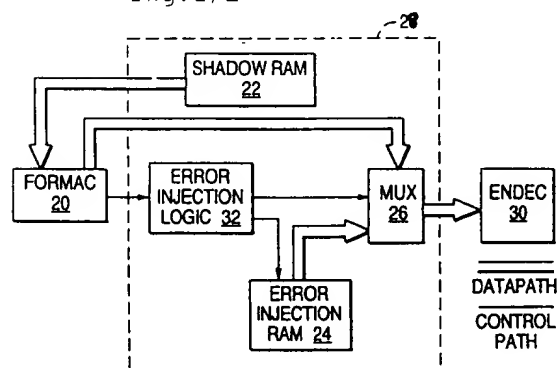US 5363379 A   6 G06F-011/00

Abstract (Basic): US 5363379 A
        The appts for injecting errors into a FDDI token ring network uses
    an error injection scheme which operates by fooling a FORMAC into
    thinking it sent a real frame of data, using **two** **RAM** buffers. The
    RAM buffer normally accessed by the RBC/DPC becomes a SHADOW RAM
    during error injection operation. A dummy frame is loaded into the
    shadow RAM in order to fool the FORMAC. The data is just like the data
    that would be used if sending a normal frame, with the restriction that
    it must be shorter than the error injection data.
        The **other** buffer, the error injection **RAM** , contains the error
    injection frame. The error injection data is sent out to the media by
    switching a **multiplexer** . When the FORMAC is done transmitting the
    data, the **multiplexer** is switched back to the normal mode. Thus, the
    FORMAC is unaware of what happened and the token ring remains
    operational.
        USE/ADVANTAGE - Injecting data frames containing errors onto fibre
    optic distributed data interface (FDDI) token ring network.
        Dwg.1/2

Title Terms: FIBRE; OPTICAL; DISTRIBUTE; DATA; INTERFACE; NETWORK; TEST;
  ADAPT; ERROR; INJECTION; CIRCUIT; INJECTION; ERROR; FDDI; NETWORK;
  VERIFICATION; OPERATE; FDDI; INTERFACE; CAN; OPERATE; NETWORK; NODE; MAC;
  IDENTIFY
Derwent Class: T01; W01
International Patent Class (Main): G06F-011/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G07; W01-A03A3; W01-A06A; W01-A06B2; W01-A06C1;
  W01-A06D

 7/19/14   (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010064899   **Image available**
WPI Acc No: 1994-332610/199441
XRPX Acc No: N94-261151
  **Reading data bits from memory for testing purposes - receiving check bits
  and multi-bit word from computer memory and generating syndrome based on
  detected data errors**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: GOODWIN P M; SMELSER D W; TATOSIAN D A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5357529	A	19941018	US 92872977	A	19920424	199441	B

Priority Applications (No Type Date): US 92872977 A 19920424
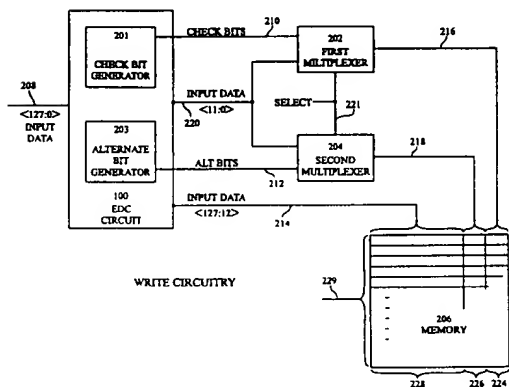Patent Details:

Abstract (Basic): US 5357529 A
        The method involves using **error   detection** and correction (EDC)
    circuitry, **multiplexers** , and a memory with first storage bits,
    second   storage bits, and third **storage** bits. In writing data to
    the memory, a multi-bit data word having a first group of data bits and
    a second group of data bits is first received from a CPU bus. The first
    group of bits is written to the first storage bits. In a ''normal''
    mode, the second group of bits is written to the **second   storage**
    bits. A set of check bits are calculated by the EDC circuit and written
    to the third storage bits. In the ''swap'' mode, the second group of
    data bits is stored in the third storage bits.
        ''Alternate'' bits are calculated by the EDC circuit, and written
    to the **second   storage** bits. In **memory** reads, contents of all of
    the storage bits are received from the memory and directed to the
    error   detecting circuit. The contents of the first storage bits are
    directed to error correction circuit. In the normal mode, the contents
    of the **second   storage** bits are directed to the error correction
    circuit; this data is corrected if necessary, and placed on the CPU
    bus. In the swap mode, the contents of the third storage bits are
    supplied to the error correcting circuit and, along with the contents
    of the first storage bits, placed on the CPU bus without error
    correction.
        ADVANTAGE - Tests computer memory check bits without introducing
    delay into read operations.
        Dwg.2/3

Title Terms: READ; DATA; BIT; MEMORY; TEST; PURPOSE; RECEIVE; CHECK; BIT;
   MULTI; BIT; WORD; COMPUTER; MEMORY; GENERATE; SYNDROME; BASED; DETECT;
   DATA; ERROR
Index Terms/Additional Words: ERROR; DETECTION; AND; CORRECTION; EDC
Derwent Class: T01; U14; U21
International Patent Class (Main): H03M-013/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G01A; U14-D02; U21-A06

 7/19/15   (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009031269   **Image available**
WPI Acc No: 1992-158629/199219
XRPX Acc No: N92-117950
   Majority signals selector - processes most and least significant digit
   places of code data separately with majority parity   testing
Patent Assignee: MOSC VOSKHOD TOOLS (MOVO-R)
Inventor: TIMONKIN G N; TKACHENKO S N; TKACHENKO V A
Number of Countries: 001 Number of Patents: 001
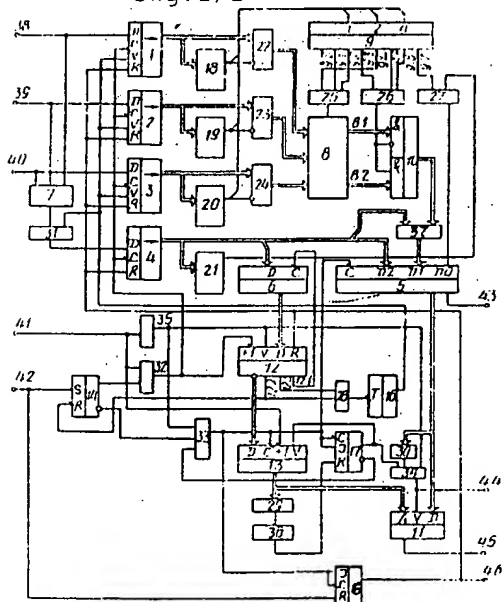Patent Family:

Abstract (Basic): SU 1656539 A
      Appts. comprises right-shift registers (1-4), storage registers
   (5,6), majority element (7), ave. value calculator (8), decoder (9),
   commutator (10), **multiplexer** (11), counters (12,13), triggers
   (14-17), mod-2 adders (18-21), AND-gates (22-24), OR-gates (25-30),
   AND-gates (31-34), delay element (25), univibrator (36), OR-gates (37)
   and inputs and outputs (38-46).
      When register (4) has received all K most significant digits of
   the data contg. data on the length of the whole piece, a pulse appears
   on the output of counter (12) at the instant that the synchronising
   pulse shifted by delay element (35) acts on the counter input. When the
   counter (12) value becomes equal to the length of the first part of the
   data, it forms a single pulse which passes via OR-gate (28) to flip
   trigger (16). This in turn closes AND-gate (31) and opens registers
   (1-3) to receive data from inputs (38-40). Then the second part of the
   data from both channels is entered in registers (1-3) and register (4)
   continues to shift data right with zeroes entered in the digit places
   freed left.
      USE/ADVANTAGE - Appts. relates to automation and computing and may
   be used in high accuracy standby control systems esp. in service and
   measuring data processing and transmission systems. Accuracy is
   increased by the introduction of four right-shift registers, **two
   storage** registers, ave. value calculator, decoder, commutator,
   multiplexer , two counters, three triggers, four mod-2 adders, three
   AND-gates, four OR-gates, two AND-gates, block of OR-gates, delay
   element and univibrator. Bul. 22/15.6.91
         Dwg.1/1

Title Terms: MAJORITY; SIGNAL; SELECT; PROCESS; SIGNIFICANT; DIGITAL; PLACE
   ; CODE; DATA; SEPARATE; MAJORITY; PARITY; TEST
Derwent Class: T01
International Patent Class (Additional): G06F-011/18; H05K-010/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G01A1; T01-G03

008813901   **Image available**
WPI Acc No: 1991-317914/199143
XRPX Acc No: N91-243634
   Semiconductor memory having error correction circuit - has multiplexers
   on outputs of memory blocks holding information and test **bits, and**
   parity   test **circuits responding to** multiplexers
Patent Assignee: HITACHI LTD (HITA)
Inventor: AOKI M; HORIGUCHI M; ITOH K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5056095	A	19911008	US 89296135	A	19890112	199143	B
KR 9300897	B1	19930211	KR 89139	A	19890107	199417	

Priority Applications (No Type Date): JP 883865 A 19880113
Patent Details:

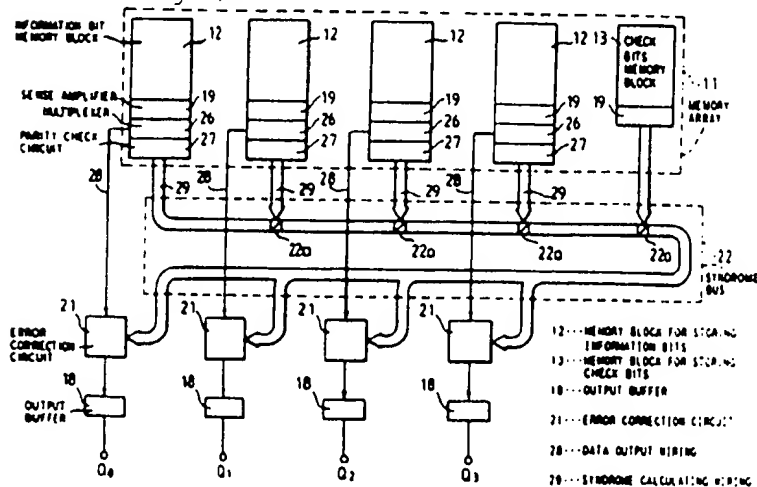| Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 9300897	B1			G11C-011/34	

Abstract (Basic): US 5056095 A
     The semiconductor memory comprises a set of memory blocks (12) for
   storing information bits, **another memory** block (13) for storing
   test bits, set of **multiplexers** (26) disposed at the respective output
   sections of the memory blocks (12), a set of **parity test** circuits
   (26) each responding to bit information for a **parity test** which is
   generated from one output from the corresponding one of th4e
   multiplexers (26).
     A syndrome bus (22) responds to both the respective outputs of the
   parity test circuits 926) and the output of the **another memory**
   block (13), and a set of error correction circuits (31) each respond to
   both output data (28) generated from the other output of the
   corresponding one of the **multiplexers** 926) and a synchrome generated
   from the syndrome bus (22).
     ADVANTAGE - Reduces number of wirings between memory blocks and
   error correction circuits, reduces chip area.
                   Dwg.1/6

Title Terms: SEMICONDUCTOR; MEMORY; ERROR; CORRECT; CIRCUIT; **MULTIPLEX** ;
   OUTPUT; MEMORY; BLOCK; HOLD; INFORMATION; TEST; BIT; PARITY; TEST;
   CIRCUIT; RESPOND; **MULTIPLEX**
Derwent Class: U14; U21
International Patent Class (Main): G11C-011/34
International Patent Class (Additional): H03M-013/00
File Segment: EPI
Manual Codes (EPI/S-X): U14-D02; U21-A06

   7/19/17   (Item 17 from file: 350)

008404651   **Image available**
WPI Acc No: 1990-291652/199039
Related WPI Acc No: 1989-017004; 1992-058420; 1992-301762; 1997-300624;
  1998-002152
XRPX Acc No: N90-224538
Cell switching system for time division multiplexers **- using common
cell memory buffer and cell address storage to detect write and chain
breaking errors**
Patent Assignee: HITACHI LTD (HITA); HITACHI KK (HITA); GOHARA S
  (GOHA-I); HORIKI A (HORI-I); KATO T (KATO-I); KUWAHARA H (KUWA-I); MORI M
  (MORI-I); OHTSUKI K (OHTS-I); SAKURAI Y (SAKU-I); AIKI K (AIKI-I); AOKI K
  (AOKI-I); ITO Y (ITOY-I); KOZAKI T (KOZA-I); YANAGI J (YANA-I)
Inventor: GOHARA S; KOZAKI T; SAKURAI Y; HORIKI A; KATO T; KUWAHARA H; MORI
  M; OHTSUKI K; AIKI K; AOKI K; ITO Y; YANAGI J
Number of Countries: 005 Number of Patents: 020
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 388648	A	19900926	EP 90103343	A	19900221	199039	B
JP 2220532	A	19900903	JP 8940230	A	19890222	199041	
US 5124977	A	19920623	US 90482090	A	19900220	199228	
EP 388648	A3	19920122	EP 90103343	A	19900221	199322	
EP 388648	B1	19970122	EP 90103343	A	19900221	199709	
DE 69029755	E	19970306	DE 629755	A	19900221	199715	
			EP 90103343	A	19900221		
US 5710770	A	19980120	US 88218217	A	19880713	199810	
			US 90482090	A	19900220		
			US 91745466	A	19910814		
			US 92845668	A	19920304		
			US 94306978	A	19940916		
			US 95462532	A	19950605		
US 5799014	A	19980825	US 90482090	A	19900220	199841	
			US 91745466	A	19910814		
			US 92845668	A	19920304		
			US 94306978	A	19940916		
US 6016317	A	20000118	US 88218217	A	19880713	200011	
			US 90482090	A	19900220		
			US 91745466	A	19910814		
			US 92845668	A	19920304		
			US 94306978	A	19940916		
			US 95462269	A	19950605		
US 36716	E	20000530	US 88218217	A	19880713	200033	
			US 90482090	A	19900220		
			US 95430809	A	19950426		
US 36751	E	20000627	US 88218217	A	19880719	200036	
			US 90482090	A	19900220		
			US 91745466	A	19910814		
			US 92845668	A	19920304		
			US 95430802	A	19950426		
US 6215788	B1	20010410	US 88218217	A	19880713	200122	
			US 90482090	A	19900220		
			US 92845668	A	19920304		
			US 94306978	A	19940916		
			US 95462269	A	19950605		
			US 99292985	A	19990416		
US 20010005386	A1	20010628	US 88218217	A	19880713	200138	
			US 90482090	A	19900220		
			US 92845668	A	19920304		
			US 94306978	A	19940916		
			US 95430802	A	19950426		
			US 95430809	A	19950426		
			US 95462269	A	19950605		
			US 99292985	A	19990416		
			US 2000725241	A	20001129		
US 6285675	B1	20010904	US 88218217	A	19880713	200154	
			US 90482090	A	19900220		

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                              Cont of application US 92845668
                              Cont of application US 94306978
                              Cont of application US 95462532
                              CIP of patent US 4910731
                              Cont of patent US 5124977
                              Cont of patent US 5365519
                              Cont of patent US 5710770
                              Cont of patent US 5799014
US 6339596    B1    H04L-012/56   CIP of application US 88218217
                              CIP of application US 90482090
                              Cont of application US 92845668
                              Cont of application US 94306978
                              CIP of patent US 4910731
                              CIP of patent US 5124977
                              Cont of patent US 5365519
                              Cont of patent US 5799014
US 6396831    B1    H04L-012/56   CIP of application US 88218217
                              CIP of application US 90482090
                              Cont of application US 92845668
                              Cont of application US 94306978
                              Cont of application US 95462532
                              Cont of application US 97925050
                              CIP of patent US 4910731
                              CIP of patent US 5124977
                              Cont of patent US 5365519
                              Cont of patent US 5710770
                              Cont of patent US 5799014
US 6445703    B2    H04L-012/56   CIP of application US 88218217
                              CIP of application US 90482090
                              Cont of application US 92845668
                              Cont of application US 94306978
                              Cont of application US 95462269
                              Cont of application US 99292985
                              CIP of patent US 4910731
                              CIP of patent US 5124977
                              Cont of patent US 5365519
                              Cont of patent US 5799014
                              Cont of patent US 6016317
US 6546011    B1    H04L-012/56   CIP of application US 88218217
                              CIP of application US 90482090
                              Cont of application US 92845668
                              Cont of application US 94306978
                              Cont of application US 95462269
                              Cont of application US 99228748
                              CIP of patent US 4910731
                              CIP of patent US 5124977
                              Cont of patent US 5365519
                              Cont of patent US 5799014
                              Cont of patent US 6016317
                              Cont of patent US 6285675
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Abstract (Basic): EP 388648 A
    A switching system handles a numbers of communication cells, each of which has a header section deifning its destination and also a data section. Cells arrive over incoming highways (1) and are transmitted on outgoing highways (6) in accordance with the cell header information. The cells are held in a common buffer memory (5) while a **second memory** (4) **stores** the addresses of empty cells. Read and wi)write operations of the common memory are controlled (3) by the empty address memory. **Errors** are **detected** by a number of units (20, 22, 24-27, 30-34).
    USE/ADVANTAGE - Provides **detection** of **errors** promptly and hence a rapid re-initialisation of the system.
    Dwg.1/17
Abstract (Equivalent): EP 388648 B
    A switching system for handling a plurality of cells, each cell including a header section and a data section, and for exchanging a communication message contained in the data section of the cell between

a plurality of incoming highways (1N) and a plurality of outgoing highways (OUT) according to the data contained in the header section of the cell, comprising: means (1) for **multiplexing** said incoming highways (1N) in time division; first memory means (5) having addressable storage locations for storing cells received from said **multiplexing** means (1); means (6) for demultiplexing and distributing data output from said first memory means (5) among said plurality of outgoing highways (OUT); **second memory** means (4) for storing an empty address of an empty storage location of the first memory means (5); and means (3) for controlling the write and read operations of said first memory means in accordance with an empty address stored in the **second memory** means used as write and read addresses; characterised by further comprising means (20,22,24-27,30-34) for **detecting** an **error** in at least one of the write address and read address and producing an error signal.
　　　Dwg.1/17

Abstract (Equivalent): US 5710770 A
　　　The system has a switch unit (1) including input ports and output ports having the same cell transmission rate. A **multiplexer** (12) **multiplexes** cell trains outputted from output ports into a single cell train, and outputs the train to a high-speed output line (and/or demultiplexer for outputting cell trains to low-speed output lines). The switch unit includes a buffer memory (11) for temporarily storing cells inputted while forming a queue chain for each line to which each cell is to be outputted.
　　　A demultiplexer (13) distributes the cells read from the buffer memory among the output ports in circulation. A circuit (10) controls the write and read operation of cells with the buffer memory, using a control table device.
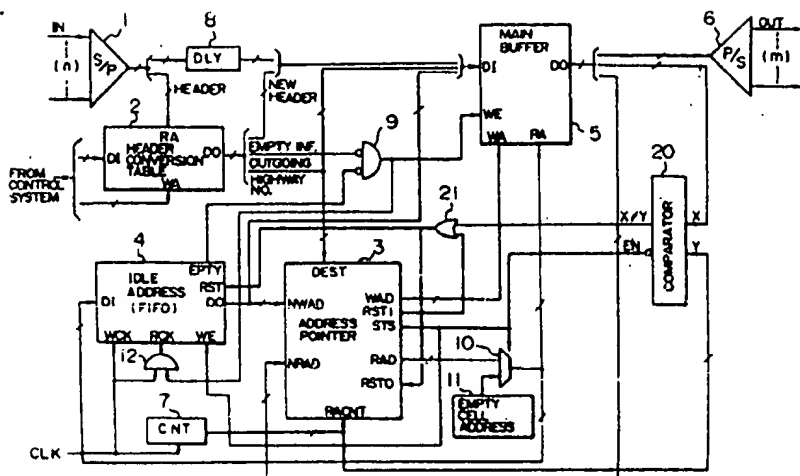　　　ADVANTAGE - Cell switching operation is in accordance with cell transmission rate of output line to be accommodated. Output lines can be of different transmission rates, e.g. 600 Mbps. 150 Mbps and 50 Mbps.
　　　Dwg.2/11
　　　US 5124977 A
　　　The switching system handles a number of cells, each including a header section and a data section, and exchanges a communication message contained in the data section of the cell between a number of incoming highways and a number of outgoing highways according to the data contained in the header section of the cell. The switching system includes a unit for **multiplexing** the incoming highways in time division, a first memory having addressable storage locations for storing cells received from the **multiplexing** unit. A unit demultiplexes and distributes data output from the first memory among a number of outgoing highways. A **second memory stores** an empty address of an empty storage location of the frst memory. A unit controls the write and read operations of the first memory in accordance with an empty address stored in the **second memory** used as write and read addresses. An **error** is **detected** in a least one of the write address and read address. ADVANTAGE - Automatically **detects error** in write or read address for main buffer.
　　　(Dwg.1/17

Title Terms: CELL; SWITCH; SYSTEM; TIME; DIVIDE; **MULTIPLEX** ; COMMON; CELL;
   MEMORY; BUFFER; CELL; ADDRESS; STORAGE; DETECT; WRITING; CHAIN; BREAK;
   ERROR
Derwent Class: W01; W02
International Patent Class (Main): H04L-012/28; H04L-012/56; H04Q-011/00;
   H04Q-011/04
International Patent Class (Additional): H04J-003/02; H04L-012/50
File Segment: EPI
Manual Codes (EPI/S-X): W01-A03A2; W01-A06X; W01-A07; W02-K09

 7/19/18   (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007851208   **Image available**
WPI Acc No: 1989-116320/198916
   **Control circuit for FIFO memory - has storage registers to temporarily
   store output from counters for reloading if error occurs**
Patent Assignee: NORTHERN TELECOM LTD (NELE   )
Inventor: CIANCIBELLO C A; GEADAH Y A; LEFEBVRE M C; CIANCIBELL C A
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 312239	A	19890419	EP 88309253	A	19881005	198916	B
US 4873666	A	19891010	US 87108655	A	19871015	198950	
CN 1035382	A	19890906				199028	
CA 1286421	C	19910716				199133	
EP 312239	B1	19960508	EP 88309253	A	19881005	199623	
DE 3855274	G	19960613	DE 3855274	A	19881005	199629	
			EP 88309253	A	19881005		

Priority Applications (No Type Date): CA 549274 A 19871014; US 87108655 A
   19871015
Cited Patents: A3...9107; No-SR.Pub; US 4616338; WO 8400835
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 312239	A	E	14		

   Designated States (Regional): DE FR GB IT NL SE

US 4873666	A		11		
EP 312239	B1	E	13	G06F-005/06	

   Designated States (Regional): DE FR GB IT NL SE

DE 3855274	G			G06F-005/06	Based on patent EP 312239

Abstract (Basic): EP 312239 A
      A write counter (217) and a read counter (218) are clocked by a
   clock signal (A). The output of the write counter including the
   overflow bit is applied to a **multiplexer** (219) register (243) and
   comparator (251). The output of the read counter is applied to the
   other input (A) of the **multiplexer** , to a further register (244) and

to a further comparator (241) of which the other input comes from the
output of the write counter register (243).
      The comparator operate for indicating the full condition or the
empty condition of the memory. The storage registers (243, 244) are
able to reload the respective write counter, read counter if an error,
such as a **parity errors**, is **detected** on the message.
      ADVANTAGE - No up-down counter, with its attendant complexity, is
required. Re-writing and re-reading section of memory can be achieved.
(14pp Dwg.No.3/4

Abstract (Equivalent): EP 312239 B
      A control circuit for a FIFO (first in first out) memory circuit
for providing address information (224) to a FIFO memory means (212)
having an address field of n bits, the control circuit comprising means
(217, 243) for generating a write address signal, means (218, 244) for
generating a read address signal, and means (219) for selecting one or
other of the write address signal and the read address signal as the
address information for the FIFO memory means, characterised by: the
write address and the read address signals having n + 1 bits of which
the n least significant bits are output by the means (219) for
selecting as the address information for the FIFO memory means; a first
comparator (248) for comparing the most significant bit of the write
address signal with the most significant bit of the read address signal
whereby to generate a first comparison signal (249) indicative of
equality or non-equality of said most significant bits; a second
comparator (251) for comparing the n least significant bits of the
write address signal with the n least significant bits of the read
address signal whereby to generate a second comparison signal (252)
indicative of equality or non-equality of said least significant bits;
and logic means (253) responsive to the first comparison signal
indicating non-equality and the second comparison signal indicating
equality, for generating a signal (247) indicative of the memory means
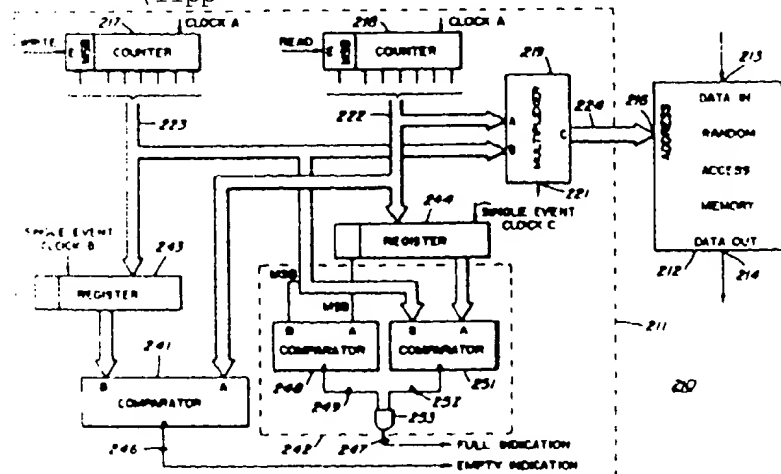being full.
      (Dwg.3/4)

Abstract (Equivalent): US 4873666 A
      A FIFO (first in first out) control circuit for providing address
information to a FIFO memory uses two up counters one to provide the
write address and one to provide the read address. A **multiplexer**
selects which address (read or write) are used. **Two storage**
registers are used to temporarily "hold" the output from the counters.
This enables the counters to be re-loaded with their original "count"
to enable either a re-reading or a re-writing of a message stored in
the FIFO memory.
      Comparators and logic circuitry are used to provide two status
output signals, namely full (or not) and empty (or not).
      (11pp

Title Terms: CONTROL; CIRCUIT; FIFO; MEMORY; STORAGE; REGISTER; TEMPORARY;
    STORAGE; OUTPUT; COUNTER; RELOAD; ERROR; OCCUR
Derwent Class: T01
International Patent Class (Main): G06F-005/06
International Patent Class (Additional): G11C-005/00; G11C-007/00;

007565278   **Image available**
WPI Acc No: 1988-199210/198829
XRPX Acc No: N88-152023
**Diagnosing and testing performance of interface module - connecting PCM
transmission path of digital TDM telephone exchange to exchange with
voice memory**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: JUGEL A; MARTIN H; STEIS B; STTEIS B
Number of Countries: 013 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 274653	A	19880720	EP 87117979	A	19871204	198829	B
BR 8706853	A	19880726				198835	
FI 8705541	A	19880618				198842	
EP 274653	B	19910807				199132	
DE 3772024	G	19910912				199138	
FI 88984	B	19930415	FI 875541	A	19871216	199320	
DK 167792	B	19931213	DK 876611	A	19871216	199404	

Priority Applications (No Type Date): DE 3643099 A 19861217
Cited Patents: 2.Jnl.Ref; A3...8831; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 274653	A	G	7		

   Designated States (Regional): AT BE CH DE FR GB IT LI NL SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 274653	B				

   Designated States (Regional): AT BE CH DE FR GB IT LI NL SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FI 88984	B			H04M-003/24	patent FI 8705541
DK 167792	B			H04M-003/24	patent DK 8706611

Abstract (Basic): EP 274653 A
     Test circuits including their following fault counters, voice
memory (SM), and the computer interface (DB/CR) are subjected to
routine tests during the unchanged continuing correct operation of the
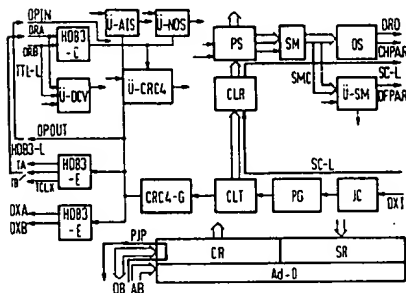interface module (FAV). The test circuits receive signals simulating
faults.
     When a test circuit responds as though in the presence of a real
fault, the fault in that function is recorded in a state register (SR)
and the fault counter is moved on but none of the events that would
occur in the presence of a real fault are initiated.
     2/2
Abstract (Equivalent): EP 274653 B
     Method for diagnosing and testing an interface unit for connecting
a PCM transmission link of a digital time-division **multiplex**
telecommunication system to an exchange in a telecommunication system,
which, in addition to **other** components, exhibits a speech **memory**
for adapting the timing of the pulse frame formed on the transmission
link to the pulse frame on which the operation of the exchange is
based, which itself is furthermore equipped with a number of monitoring
circuits evaluating different criteria of the information transmission
on the PCM link, which are at least partially associated with error
counters, and which is connected to a separate control system via a
computer interface, characterised in that the test circuits (U-AIS,
U-NOS, U-DCV, U-CRC4, U-SM) and subsequent error counters, the speech
memory (SM) and the computer interface (DB/CR) are subjected to routine
tests during the proper operation of the interface unit (FAU) which
continues unchanged, for which purpose, apart from the criteria to be
monitored by them, simulation quantities corresponding to an error are
applied to the test circuits under control by the control system, in

which connection in each case when the test circuits are operated as in the case of the presence of an actual error of the function to be monitored, a fault indication occurs in a state register (SR) or an incrementing of the error counter occurs, but none of the measures provided for the case of the presence of an actual error is taken, for whcih purpose, furthermore, in the speech memory (SM), the information to be entered is provided with a parity bit field related either ine ach case to a channel-individual memory cell and after a reading-out is subjected to a **parity check** (U-SM), or, under control by a higher-priority control system of the exchange, after a switching-related blocking of the relevant channel, a bit pattern normally sent from the exchange as idle-channel code word is switched to the relevant speech mem

Title Terms: DIAGNOSE; TEST; PERFORMANCE; INTERFACE; MODULE; CONNECT; PCM; TRANSMISSION; PATH; DIGITAL; TDM; TELEPHONE; EXCHANGE; EXCHANGE; VOICE; MEMORY
Derwent Class: W01
International Patent Class (Main): H04M-003/24
International Patent Class (Additional): H01J-003/14; H04J-003/14; H04Q-001/20; H04Q-011/04
File Segment: EPI
Manual Codes (EPI/S-X): W01-B07; W01-C02A1

 7/19/20   (Item 20 from file: 350)

007329873
WPI Acc No: 1987-326880/198746
XRPX Acc No: N87-244406
  Computing self-monitoring modular memory - has codes of two error locators compared to form output signal through OR-gate signalling correctable error in one module
Patent Assignee: MOSC POWER INST (MOPO)
Inventor: BORODIN G A; STOLYAROV A K
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1302329	A	19870407	SU 4004952	A	19851230	198746	B

Priority Applications (No Type Date): SU 4004952 A 19851230
Patent Details:
Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 1302329	A		5		

Abstract (Basic): SU 1302329 A
     The memory contg. **two** control bits forming circuit for **memory** modules with outputs to another two control bit forming circuits, an error corrector, **multiplexer** , bit -by-bit comparator, comparator and an error locator, has the control bit forming circuits (19,18) comparator (23) code comparators (24,25), comparator (26), error locator (28) NOT-gates (29) switch (30) OR-gates (31,32) and AND-OR-gate (33).
     USE/ADVANTAGE - In computing technique for a self-monitoring memory

to **detect** unidirectional **errors** in **two** **memory** modules and to
correct unidirectional errors in one memory module, monitoring is more
certain and information capacity is increased. The number of word
digits is doubled. The ordinal numbers of failed memory modules are
encoded. Bul.13/7.4.87 (5pp Dwg.No.1/5)
Title Terms: COMPUTATION; SELF; MONITOR; MODULE; MEMORY; CODE; TWO; ERROR;
  LOCATE; COMPARE; FORM; OUTPUT; SIGNAL; THROUGH; OR-GATE; SIGNAL; CORRECT;
  ERROR; ONE; MODULE
Derwent Class: U14
International Patent Class (Additional): G11C-029/00
File Segment: EPI
Manual Codes (EPI/S-X): U14-D02

 7/19/21   (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007329871
WPI Acc No: 1987-326878/198746
XRPX Acc No: N87-244404
  Computing modular error correcting memory - has two error   detectors
  each forming module ordinal number when two modules fail
Patent Assignee: MOSC POWER INST (MOPO)
Inventor: BORODIN G A
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
SU 1302327   A   19870407 SU 3997905   A   19851230 198746 B

Priority Applications (No Type Date): SU 3997905 A 19851230
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
SU 1302327   A   6

Abstract (Basic): SU 1302327 A
     The circuitry contg. **two** control digit forming circuits for
  memory modules with outputs to another two control digit forming
  circuits, an error corrector, two comparators, **multiplexer** and an
  error **detector** , has the control digit forming circuits (18,19).
  Berger code forming circuits, two more comparators, another **error**
  detector and a type of error finder.
     USE/ADVANTAGE - In computing as memory with self-monitoring by
  detection of modular unidirectional **errors** in **two** **memory** modules
  and their correction in one, monitoring is more certain. The presence
  of the two errors is determined by comparison. The codes of the ordinal
  numbers of the failed modules are formed by two detectors. The third
  detector forms a signal for correction and an incorrectible error
  signal. Bul.13/7.4.87 (6pp Dwg.No.1/6)
Title Terms: COMPUTATION; MODULE; ERROR; CORRECT; MEMORY; TWO; ERROR;
  DETECT; FORMING; MODULE; ORDINAL; NUMBER; TWO; MODULE; FAIL
Derwent Class: U14
International Patent Class (Additional): G11C-029/00
File Segment: EPI
Manual Codes (EPI/S-X): U14-D02

 7/19/22   (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007085616
WPI Acc No: 1987-085613/198712
XRPX Acc No: N87-064280
  **Memory units tester - uses arithmetic unit to form current data for input
  to** multiplexer **via register**
Patent Assignee: KIEV ELTRN COMPUTER (KIEL-R)
Inventor: BELALOV F Y A; BOCHKOV V K; PUDAKOV E V

Number of Countries: 001   Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
SU 1247951   A   19860730 SU 3878097   A   19850226 198712 B

Priority Applications (No Type Date): SU 3878097 A 19850226
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
SU 1247951   A   6

Abstract (Basic): SU 1247951 A
        The appts. includes control unit (2) arithmetic unit (1) two
    comparators (6,7) and six registers (17-22). For faster response it is
    further equipped with accumulators (3-5) **multiplexers** (10-16) further
    registers (23-30), counter (31), decoder (8) signals shaper (9),
    parity   tester (32), two switches (33,34) and indicators (35-37).
        The arithmetic unit (1) analyses initial parameters which are
    received through the registers (26-30) through the **multiplexer** (12)
    and a current access address to a tested unit is formed. Results of
    operation of the arithmetic unit (1) and the **other** data are stored in
    the **memory** of said unit. A current address from the arithmetic unit
    is transferred to the register (19) the **multiplexer** (14) and through
    the **multiplexer** (15) to the register (20) the comparator (7) compares
    the present (current) address with the final address.
        USE - In computer engineering for tuning and testing operational
    and peripheral memories. Bul. 28/30.7.86
        Dwg.1/2
Title Terms: MEMORY; UNIT; TEST; ARITHMETIC; UNIT; FORM; CURRENT; DATA;
   INPUT; **MULTIPLEX** ; REGISTER
Derwent Class: U14
International Patent Class (Additional): G11C-029/00
File Segment: EPI
Manual Codes (EPI/S-X): U14-D03

 7/19/23   (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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003352140
WPI Acc No: 1982-L0162E/198233
  **Memory with self checking facility - has control signals former
  comparator and** multiplexer **coupled to register**
Patent Assignee: MOSC POWER INST (MOPO)
Inventor: BORODIN G A; EGOROVA N I; OGNEV I V
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
SU 875456   B   19811023   198233 B

Priority Applications (No Type Date): SU 2883225 A 19800214
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
SU 875456   B   5

Abstract (Basic): SU 875456 B
        Memory with self-checking facility uses a **second   store** , control
    signals former, comparator and multiplier to increase effective
    capacity. Binary codes are applied directly to the first store (1) with
    checking codes stored in the first group parity signal formers (3,4).
    Checking digits are formed by adding weighting marks to the formers'
    code.
        During read-out, the store (1) data are transferred to the output
    register (6) and the second group parity signals former (7). Parity
    codes are compared for **detecting** storage **errors** . Faulty cell
    address is discriminated by using a **second** comparator (10) and **store**
    (2). Permanent **second   store** accumulates both comparators' (9,10)
    results, storing the faulty cells address code. Error correction is

effected through the **multiplexer** (5) and the numbers register (6).
Bul. 39/23.10.81. (5pp Dwg.No.1/1)
Title Terms: MEMORY; SELF; CHECK; FACILITY; CONTROL; SIGNAL; FORMER;
  COMPARATOR; **MULTIPLEX** ; COUPLE; REGISTER
Derwent Class: T01; U14
International Patent Class (Additional): G11C-011/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-H; U14-A20; U14-D

 7/19/24   (Item 24 from file: 350)

002353372
WPI Acc No: 1980-F9821C/198028
  Error   detection **in microprocessor systems - by executing error
  routine during access period of macro-programmed memory**
Patent Assignee: STAND ELEK LOREN (INTT)
Inventor: ILLI D
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
DE 2855004   A   19800703   198028 B

Priority Applications (No Type Date): DE 2855004 A 19781220

Abstract (Basic): DE 2855004 A
      An **error   detector** routine for microprocessor systems operates
  during the accessing period required for macro-instructions and so does
  not slow down the operation of the system.
      The central processor is controlled by a micro programme store for
  executing all internal control signal generations. User data is entered
  from a **separate   memory** over a register and **multiplexer** .
  Macro-instructions, such as jump operations, are held in a programme
  store coupled over a register and first-in-first out memory. During the
  access period of the macro store, an **error   checking** operation is
  performed. Test data held in a register is delivered and transmitted to
  mask register. The generated data is **multiplexed** into a second
  register and is compared with the output to indicate any error.
Title Terms: ERROR; DETECT; MICROPROCESSOR; SYSTEM; EXECUTE; ERROR; ROUTINE
  ; ACCESS; PERIOD; MACRO; PROGRAM; MEMORY
Derwent Class: T01
International Patent Class (Additional): G06F-011/00
File Segment: EPI
Manual Codes (EPI/S-X): T01-G02

 7/19/25   (Item 25 from file: 350)

002310462
WPI Acc No: 1980-B6893C/198008
  **Checking system for integrated storage matrix - divides latter into two
  independently addressed zones with some words used as check words**
Patent Assignee: SIEMENS AG (SIEI)
Inventor: ELSNER P
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No   Kind   Date   Applicat No   Kind   Date   Week
DE 2834745   A   19800214   198008 B

Priority Applications (No Type Date): DE 2834745 A 19780808

Abstract (Basic): DE 2834745 A
      The checking system uses an auxiliary store (HS) for listing the
  addresses of storage cells where an **error** is **detected** . The store is

divided into two equal, independently addressed zones (SB1, SB2), with words read from one zone used as checks words for the words read from the storage cells of the other zone.

A checking counter (Zp) provides the addresses of the check words, with two **multiplexers** (MPX1, MPX2) for independently addressing the **two storage** zones (SB1, SB2) with the check word and an externally demanded storage word supplied to a device (F) for error recognition and correction.

Title Terms: CHECK; SYSTEM; INTEGRATE; STORAGE; MATRIX; DIVIDE; LATTER; TWO ; INDEPENDENT; ADDRESS; ZONE; WORD; CHECK; WORD
Derwent Class: U14
International Patent Class (Additional): G11C-029/00
File Segment: EPI

7/19/26   (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO
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06097713   **Image available**
MEMORY MONITORING CIRCUIT

PUB. NO.:   11-039232 [JP 11039232 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s):   HASEGAWA TOMOHIKO
APPLICANT(s): NEC ENG LTD
APPL. NO.:   09-196725 [JP 97196725]
FILED: July 23, 1997 (19970723)
INTL CLASS: G06F-012/16; G06F-012/16

ABSTRACT
PROBLEM TO BE SOLVED: To make a memory versatile and, at the same time, to simplify a constitution for monitoring the memory.

SOLUTION: Bit phase synchronizing circuits 10-1 to 10-m which respectively output the input signals to all memories 11-1 to 11-m which write (k) input signals **multiplexed** with and synchronized to N words by synchronizing the bit phases of the signals to each **other** to the **memories** 11-1 to 11-m are provided on the input sides of the memories 11-1 to 11-m. One set of circuits composed of a parity bit generating circuit 12 which generates one parity bit signal DPB by connecting the outputs of the circuits 10-1 to 10-m and adding one vertical parity to received data and stores the data DPB in a parity bit memory 14 and a **parity** bit **detecting** circuit 13 which generates a parity bit output data signal DPB by connecting the outputs of the memories 11-1 to 11-m and adding one vertical parity to all data and compares the signal DPBO with the previously stored data signal DPB can monitor the parities of the memories 11-1 to 11-m each of which does not require any larger capacity than the (k) input signals.

7/19/28   (Item 28 from file: 347)
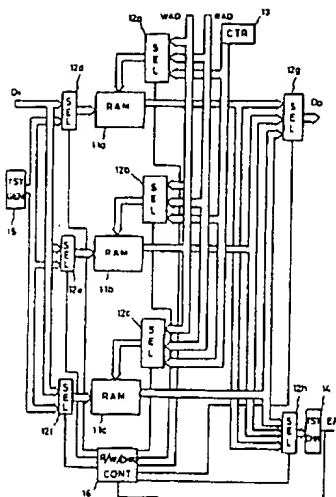DIALOG(R)File 347:JAPIO
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02955452   **Image available**
MONITORING SYSTEM FOR MEMORY

ABSTRACT
PURPOSE: To securely **detect** even a fixed **error** by writing and reading a
time- division **multiplex** signal (TDM) by using 1st and **2nd memories**
alternately, and writing and reading test pattern data (TPD) by using a 3rd
memory and checking the read TPD.
CONSTITUTION: A memory for time slot conversion is provided with the
1st-3rd memories 11a-11c, the 1st and **2nd memories** 11a and 11b are used
to write and read the TDM, and the 3rd memory 11c is used to write and read
the TPD and also check the read TPD. Then those are written and read by
being shifted to the 1st-3rd memories 11a-11c in order repeatedly.
Consequently, the respective memories can be monitored by turns and the
RAMs 11a-11c are reduced in necessary capacity and a failure in **error
detection** due to readout fixation to a normal state is eliminated.

7/19/29   (Item 29 from file: 347)
DIALOG(R)File 347:JAPIO
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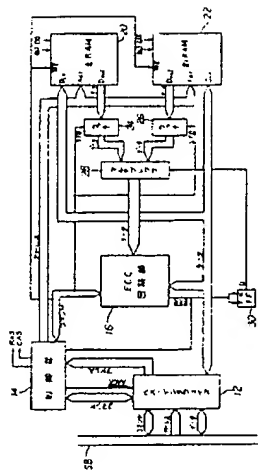
02469151   **Image available**
MEMORY DEVICE

PUB. NO.:   63-086051 [JP 63086051 A]
PUBLISHED: April 16, 1988 (19880416)
INVENTOR(s):   HIUGA SEIJI
APPLICANT(s):   TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
                (Japan)
                TOSHIBA MICRO COMPUT ENG CORP [486761] (A Japanese Company or
                Corporation), JP (Japan)
APPL. NO.:   61-232328 [JP 86232328]
FILED: September 30, 1986 (19860930)
INTL CLASS: [4] G06F-012/16
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 752, Vol. 12, No. 323, Pg. 105,
                September 02, 1988 (19880902)

ABSTRACT
PURPOSE: To ensure correction even with an error of many bits by providing
an auxiliary memory to a memory and using this auxiliary memory in place of
a part of the memory when it is detected that the information given from
the memory is wrong.

CONSTITUTION: The same data is stored in both a main ROM 20 and a
 secondary   RAM   22 together with an **error   detection**   code used for
correction of an error. A **multiplexer** 28 selects the data received from
the RAM 20 or the RAM 22 and outputs it to an ECC circuit part 16. Thus the
circuit 16 **detects** the **error** of the data selected by the **multiplexer**
28. When the number of error bits is small and the part 16 itself can
correct the error, the correction data are written again to the RAM 20 and
the RAM 22. While the data selected by the **multiplexer** 28 are changed if
the number of error bits is large.

7/19/30   (Item 30 from file: 347)
DIALOG(R)File 347:JAPIO
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01985004   **Image available**
MEMORY **MULTIPLEXING** CONTROL SYSTEM

ABSTRACT
PURPOSE: To   realize   **multiplexing**   easily   without   damaging   the
economization by cascading plural memory devices and writing and reading
the same data in and from the same addresses of all memory devices at the
same timing.

CONSTITUTION: **Error   checkers** 13, memory **multiplexing** control circuits
14, and   **multiplexing**   control   signals   6-1-6-(n-1) cascading adjacent
memory devices are provided, and the same data is written or read in and
from the same addresses of all memory devices 4-1-4-n at the same timing,
and data is written or read in or from the first memory device if the first
memory device is normal; but if data **error** is **detected**, the abnormality
of the first memory device is reported to the **second** **memory** device by a
multiplexing signal to write or read data in or from the **second** **memory**
; and if the first - the (i-1)th memory devices are abnormal, data is
written in or read from the i-th memory device. Thus, the memory
multiplexing operation is performed.